WHITE PAPER

- Clock jitter and phase noise -

1. Background

Recently, crystal oscillators, which are used in different electronic equipment including information and communications equipment, have been required to further lower the noise as well as high speed the reference clock signal along with the increase in the amount of information. Many applications require a high quality clock signal source such as the narrowing of deviations in phase noise, for the trend of an increased use of quadrature amplitude modulation systems, the improvement of resolutions of onboard millimeter-wave radars, and the faithful reproduction of original sound by DA conversion clocks for digital audio systems. Provided with excellent frequency stability, crystals or crystal oscillators incorporating them are used as high-quality signal sources for clocks in many types of electronic equipment. Crystals or crystal oscillators excel not only in long-term or static stability such as frequency stability, temperature characteristics, and ageing characteristics, but also in short-term high stability represented by the phase noise and jitter performance thanks to high Q-values of crystals .

This article gives an overview of jitter and phase noise in crystal oscillators, and introduces our products developed to address the lowering of phase noise in particular at the end.

2. Jitter and phase noise

(1) Jitter

Jitter expresses a drift from the ideal position of the clock edge occurring as the result of the fluctuation of the clock signal waveform in the direction of the time axis. The output voltage waveform of a crystal oscillator, as shown in the illustration, shows a certain fluctuation range from the position at which the waveform should be originally located in the edge section separated by one period from the trigger point. This fluctuation is called period jitter because it corresponds to the time variation of one period of the clock.

This fluctuation is generally expressed in an RMS or peak-to-peak value in the histogram. Three kinds of unit, rad, second, and unit interval (UI), are available to express a fluctuation. In most cases, however, the unit of second is generally used.

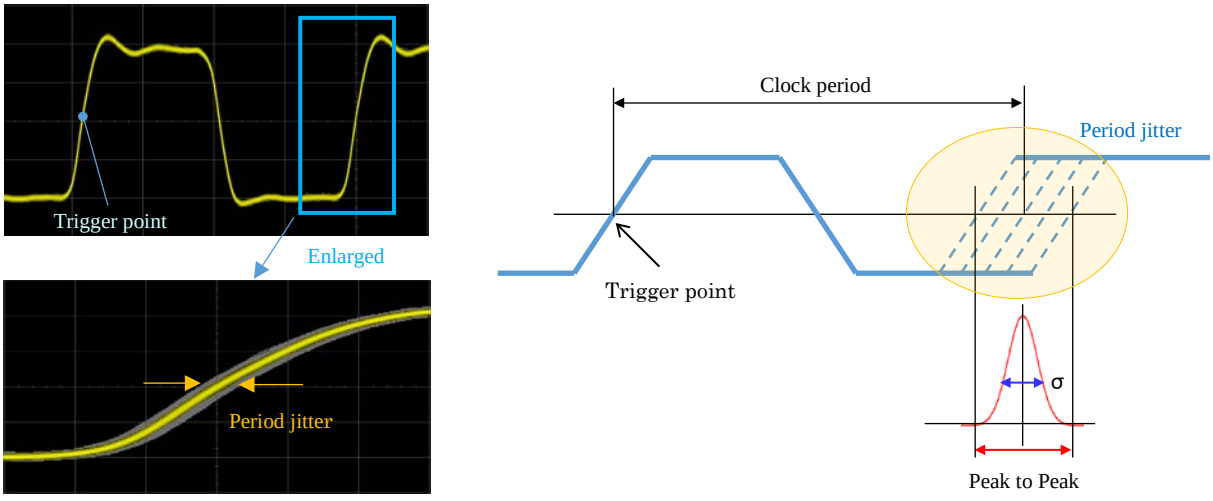

Fig. 1 Output waveform and period jitter for crystal Oscillator

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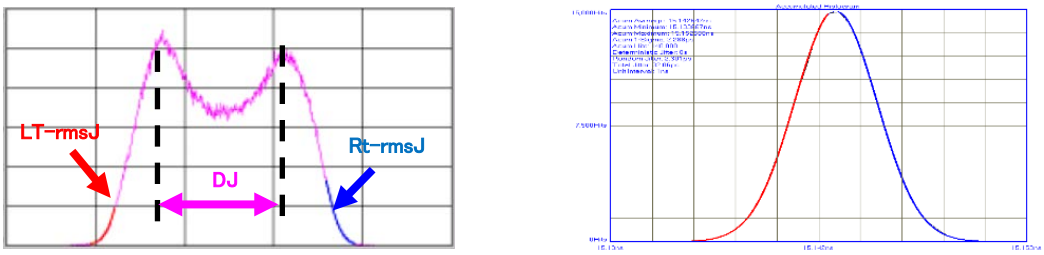
Jitter is roughly classified into random jitter (RJ) and deterministic jitter (DJ) according to the cause of its occurrence.

RJ occurs spontaneously from thermal or shot noise in semiconductor devices. Since RJ occurs as the result of accumulation of a number of minute noise generation processes, its shape of distribution approximates a normal distribution.

On the other hand, DJ is produced by various factors with regularity, such as circuit designs, electromagnetic induction and externally induced factors, being classified into periodic jitter (PJ) and data-dependent jitter (DDJ) according to the cause of its occurrence. The width of variation of its distribution has a characteristic provided with a border that can be expressed by a part sandwiched between RJ on both sides. A specific cause of occurrence that is not random exists, and the drift of the edge is not a random dispersion but a deterministic (predictable) jitter component. Combined together, RJ and DJ are called total jitter (TJ).

A crystal oscillator in which the output frequency is directly produced without using a PLL circuit has almost no DJ component, virtually having an RJ component only.



PLL oscillator　　Crystal oscillator

Fig. 2 Random jitter and deterministic jitter

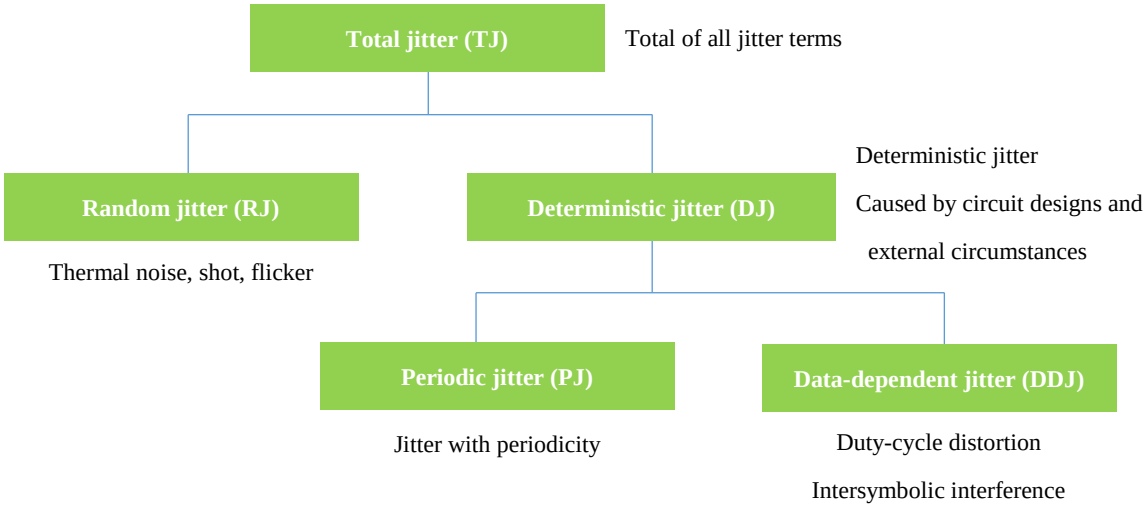
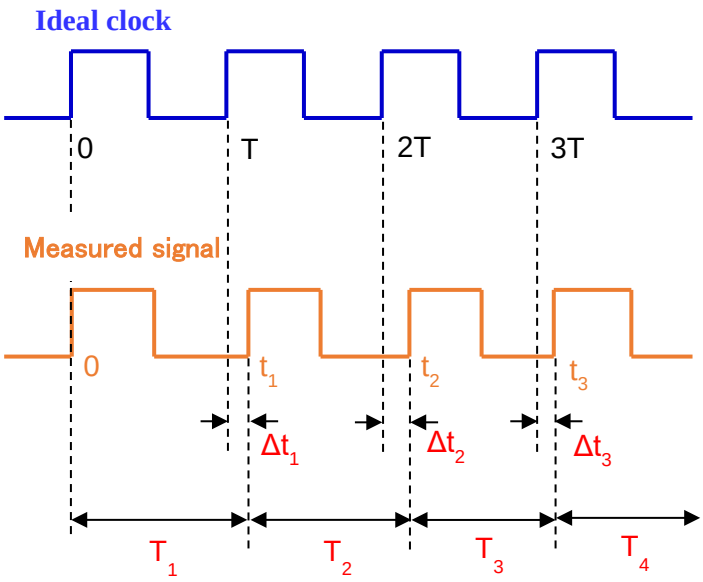


Fig. 3 Different kinds of jitter

Depending on how the jitter timing is defined, jitter is classified into phase jitter, period jitter, and intercyclic jitter. Phase jitter is an accumulation of the difference between the ideal clock of the clock edge and the measured signal, and it is called long-term jitter or accumulated jitter depending in the case. Period jitter expresses the variation in a clock period and intercyclic jitter the variation in the difference between the periods of adjoining clocks.



●Phase Jitter

The phase variation from the ideal clock

$\Delta t_n = t_n - nT$

●Period Jitter

The variation of cycle to cycle of measured signal

$T_n = t_n - t_{n-1}$

●Intercyclic jitter (Cycle to Cycle Jitter)

Variation of the difference between the periods of adjoining clocks

$T_{n+1} - T_n = (t_{n+1} - t_n) - (t_n - t_{n-1})$

Fig. 4 Phase jitter, period jitter, and intercyclic jitter

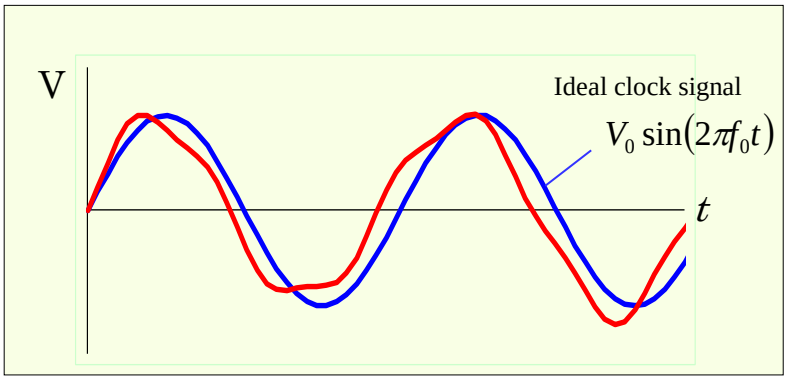
(2) Phase noise and phase jitter

Phase noise refers to the power spectrum density of phase fluctuation, providing a measure showing the purity of a signal. Phase noise is expressed by the frequency components at the location separated by a certain magnitude from the center frequency (the offset frequency), and the smaller the noise value is, the better the signal is considered to be because of the presence of fewer noise components. Phase noise is usually expressed by normalizing noise in the neighborhood of the single sideband with reference to the carrier electric power.

In Fig. 5, a signal waveform with phase noise V (t) is expressed in the form of a phase term of an ideal sinusoidal wave with the addition of phase variation Φ (t). The phase noise and the phase jitter are given by the phase variations Φ (t) obtained in the frequency domain and in the time domain.

$$V(t) = (V_0 + \varepsilon(t))\sin(2\pi f_0 t + \phi(t))$$

ε(t): Amplitude variation φ(t): Phase variation



- Instantaneous value of phase

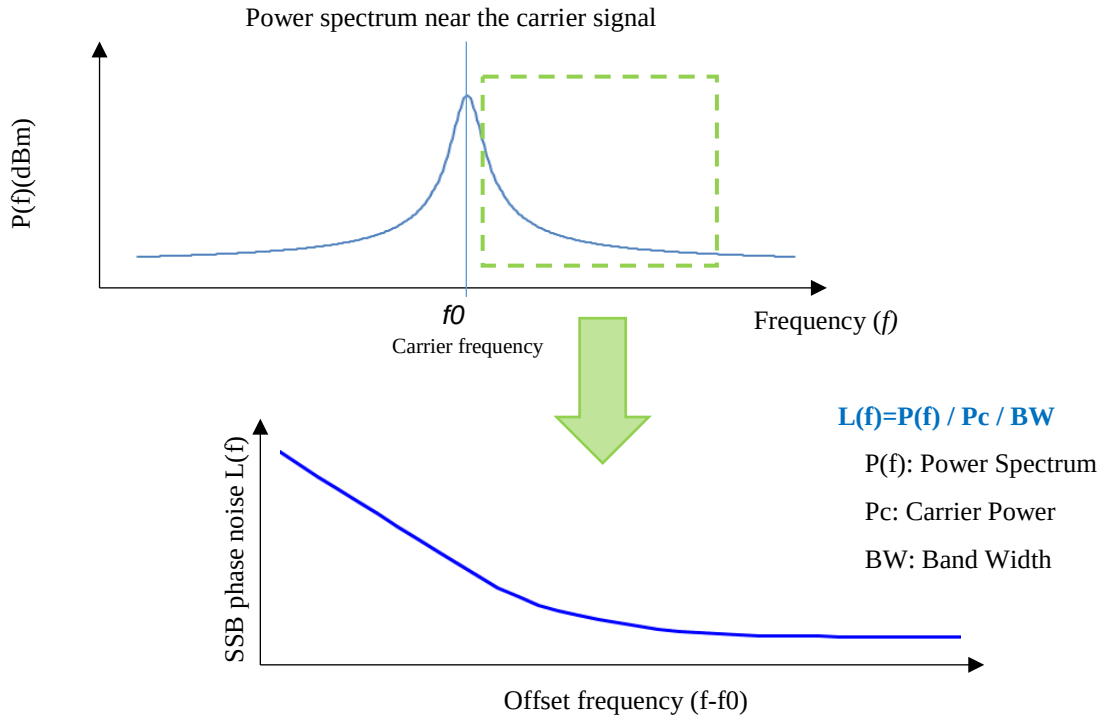
$$\Phi(t) = 2\pi\, t + \phi(t)$$

- Instantaneous value of frequency

$$f(t) = f_0 + \frac{1}{2\pi}\frac{d\phi(t)}{dt}$$

Fig. 5 Output voltage including the phase variation

Phase noise is expressed in the frequency domain of the phase variation Φ (t), being defined by the power spectrum density SΦ. In practice, single sideband (SSB) phase noise L (f) expressed in the single sideband is usually used, with the ratio of the carrier signal to the total electric power being expressed in dBc/Hz on the horizontal axis indicating the offset from the carrier frequency.



$$L(f) = \frac{\text{Power spectrum density of single sideband phase noise per Hz of band}}{\text{Total signal power}}$$

Fig. 6 SSB phase noise

On the other hand, phase jitter is an index of noise in which the phase variation is expressed on the time axis; it can be said to be the function Φ (t) itself. The RMS value of phase jitter is given by the root mean square of Φ (t) as shown below:

$$J_{rms} = \left\langle \phi^2(t) \right\rangle^{1/2}$$

Measuring Φ (t) exactly in the time domain is extremely difficult. However, a convenient method which can be used is first measuring the phase noise and then converting it into the phase jitter according to the following method.

A relationship as shown below approximately holds between the power spectrum density of phase variation SΦ and the SSB phase noise L (f) evaluated in a single sideband:

$$L(f) = S_{\varphi}(f)/2$$

Under this condition, the phase jitter can be obtained by integrating the measured value of phase noise SΦ between the interval of the designated offset band width.

$$J_{rms} = \frac{1}{2\pi f_0}\left[\int_{f_1}^{f_2} S_{\phi}(f)dt\right]^{1/2}$$

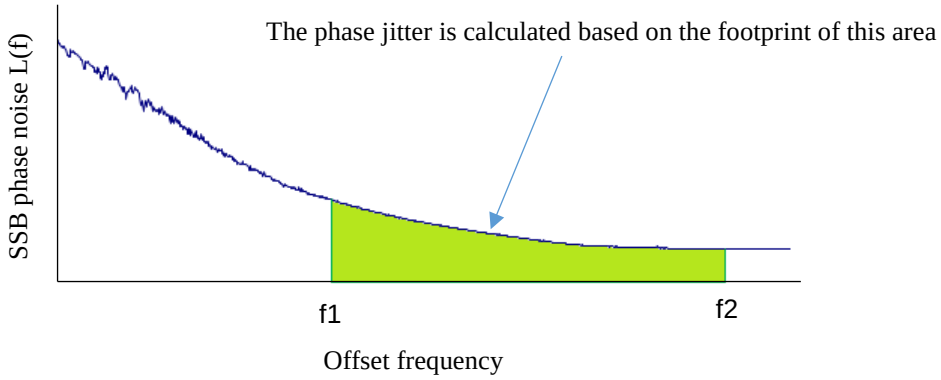


Fig.7 Calculation of phase jitter from the SSB phase noise

(3) To obtain clock signals excellent in noise performance

The main part of phase noise in a crystal oscillator is determined by the Q value and signal level of the crystal and the noise performance of the oscillation circuit. In improving the phase noise performance near the carrier frequency of phase noise, the Q value of the crystal plays a particularly important role.

The higher the signal level is, the lower the phase noise level becomes regardless of the offset frequency. Phase noise can be lowered by setting the signal level at as high a value as the system allows. However, the upper level of excitation applicable to a crystal is limited. An excessively high excitation level may cause unnecessary oscillation modes to occur, with the oscillation becoming abnormal.

Overtones help secure high Q values and hence are effective near the offset value. However, you should be careful about overtones because they cause the resistance loss in the crystal and oscillation circuit to increase and also because operating at a highly excited level allows the frequency to fluctuate greatly and thereby to degrade the frequency purity.

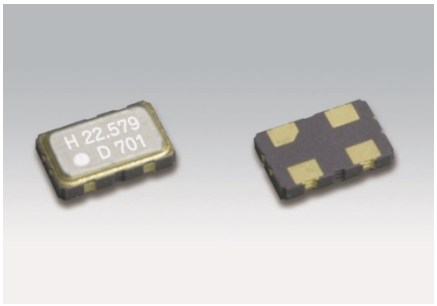
In addition, greater electric power causes the frequency fluctuation to increase due to the non-linearity of the crystal, with operation at an excessive excitation level likely to cause deterioration in the phase noise. Selecting semiconductor devices

with excellent noise performance is important. The offset frequency of flicker noise affects the frequency zone from the vicinity of the carrier frequency to the vicinity of intermediate frequencies of approximately 10 kHz, while thermal noise affects the entire offset zone in the same way as the signal levels do.

- To obtain favorable phase noise -

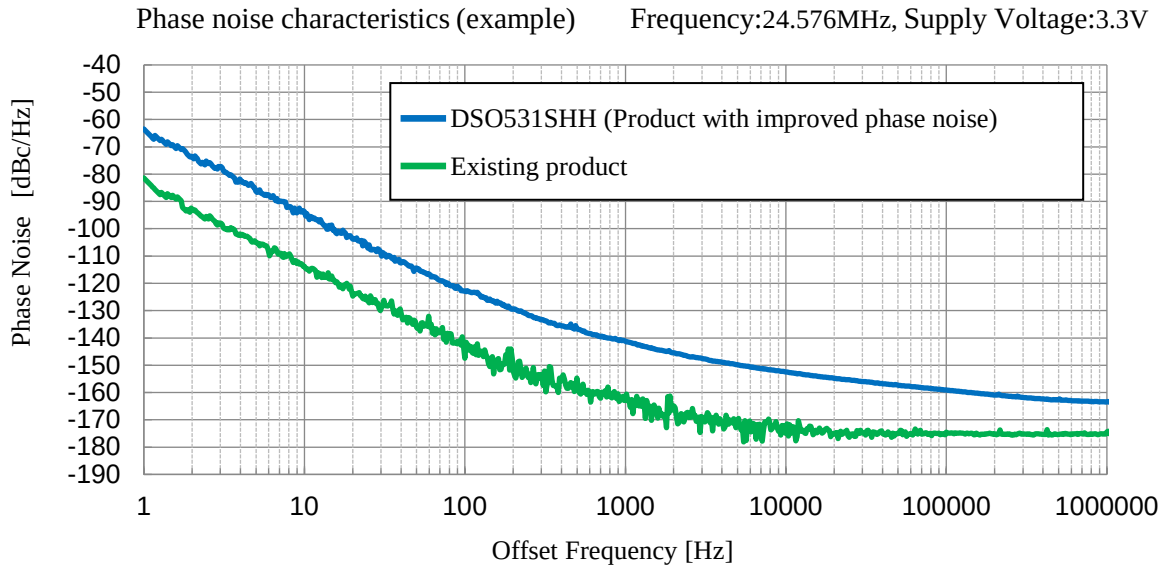
1. Secure a favorable Q value of the oscillation circuit.
   Use a crystal with a high Q value, and lower the resistance loss of the oscillation circuit to obtain Q higher in the oscillation loop.
2. Minimize the device noise.
   Select a device characterized by minimal values in noise figure (NF), and flicker corner frequency (Fc) to minimize thermal noise, shot noise, and flicker noise from the semiconductor device.
3. Do not use a frequency multiplication scheme using a PLL circuit because it causes the degradation of phase noise.
4. Enhance the drive level of the oscillator circuit as high as allowed.
5. Since the noise characteristic is a relative value of the signal level to the noise power, the higher the signal level is, the more favorable the noise characteristic is. This is, however, on condition that the crystal be used in a domain in which its drive level characteristic is flat.
6. Overtones provide a high Q value, being useful in the vicinity of the offset. Note, however, pay attention to the degradation of phase noise by the fluctuation of frequency as that overtones allow the resistance loss in the crystal and the oscillation circuit to grow and that the operation at a higher drive level increases the frequency fluctuation that leads to the deterioration of the signal purity.
7. Restrict noise from the power supply by placing bypass capacitors in the shortest distances to the power supply and the ground terminal.

◆Introduction of DSO531SHH, a new product



It is known in the field of digital audio systems that phase noise in the reference clock signal used in DACs degrades sound quality. Providing a solution to this problem, DSO531SHH, our new product, is a crystal oscillator, specialized for audio applications, excellent in noise performance. The new product adopts not only a low-noise process in the oscillation circuit, but also an IC oscillation circuit in which phase noise is minimized by optimizing the vibration level and the negative resistance in keeping with the parameters of the crystal. These innovative efforts have enabled us to reduce phase noise by 10 to 20 dB in comparison with our existing models. The circuit design has also been reviewed concerning RMS jitter, which has been reduced to approximately to 1/3 of that in existing models. This review of the design has contributed to the improvement of sound quality in digital audio equipment through the resulting excellent signal quality. The adoption of ceramic packages with a size of 5.0 x 3.2 mm (a 5032 size) has helped lower the fluctuation in signals due to thermal fluctuation and mechanical vibration in comparison with smaller ceramic packages with a size of 3.2 x 2.5 mm (a 3225 size) or 2.0 x 1.6 mm (a 2016 size) in the volume zone. In addition, the optimization of the design of crystals prevents neighborhood phase noise in the high-drive domain from deteriorating, securing stable and satisfactory characteristics over the entire band.

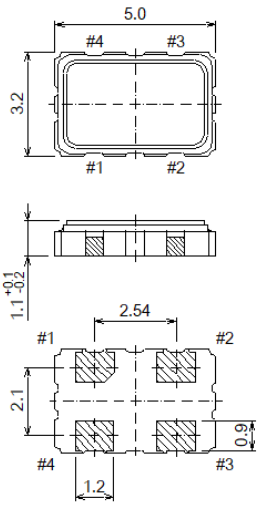
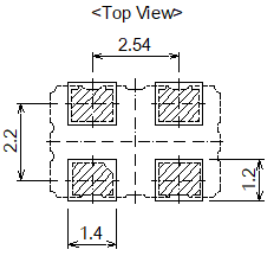
Our company will continue to develop our unique products to respond to our customers' needs.



Item	Unit	DSO531SHH (Product with improved phase noise)	Existing product	⊿ Improvement	Condition
Phase Noise	dBc/Hz	-77.9	-63.7	**-14.2**	Offset: 1Hz
		-111.5	-92.2	**-11.3**	Offset: 10
		-141.9	-123.3	**-15.1**	Offset: 100
		-159.2	-140.2	**-18.7**	Offset: 1,000
		-182	-151.4	**-21.2**	Offset: 10,000
		-175.2	-158.6	**-13.6**	Offset: 100,000
		-175.3	-162.9	**-7.7**	Offset: 1,000,000
Phase Jitter (RMS)	ps	0.07	0.27	**-0.2**	BW: 12k ～ 5MHz

Fig.8 Phase noise and Phase Jitter

Table 1: DSO531SHH Electrical specification

Item	Unit	Specification
Output Frequency Range	MHz	20 to 50
Frequency Stability	x 10^{-6}	±50 / -40 to +85℃
		±30 / -20 to +70℃
Supply Voltage	V	+ 1.8 to 3.3
Current Consumption	mA	+ 2.7 / Vcc=1.8V + 7.7 / Vcc=3.3V
Symmetry	%	45 to 55
Output Waveform		CMOS
0 Level Output Voltage / 1 Level Output Voltage		0.1 Vcc / 0.9 Vcc
Load Condition	pF	15 max.
Phase Noise (Output Frequency: 24.576MHz)	dBc/Hz	-160 typ. / Vcc=3.3V , Offset 1kHz -172 typ. / Vcc=3.3V , Offset 100kHz
		-158 typ. / Vcc=1.8V , Offset 1kHz -166 typ. / Vcc=1.8V , Offset 100kHz
Output Control		Enable / Disable Control (3-state)
Dimensions	mm	Dimensions  Pin Connections Pin No. | Connection #1 | OE(Output Enable) #2 | GND #3 | Output #4 | Vcc Recommended Land Pattern 

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