Development of Voltage-Controlled Crystal Oscillators DSV753C Series with Fundamental Oscillation Mode (AT Cut) Up to 700 MHz, Industry's Highest※

September 9, 2013

Daishinku Corporation (President: Sohei Hasegawa) is pleased to announce the development of voltage-controlled crystal oscillators, the DSV753C series, which use a fundamental oscillation mode AT-cut crystal resonator, directly outputting high frequency.

Recent increases in communications traffic call for higher-frequency, lower-noise and higher-accuracy clock signals for high-speed optical communications. Conventional high-frequency oscillators generally use a SAW device or frequency multiplication to convert fundamental frequency to higher frequency.

However, frequency multiplication produces phase noise and degrades jitter performance, as the output signal contains frequencies that are integral multiples of the oscillation frequency. Characteristic curves of frequency versus temperature in SAW devices are generally quadratic curves. If stability is required over a wide temperature range, AT cut is desirable, in which frequency-temperature characteristics are represented as cubic curves. Meanwhile, using existing techniques, the maximum available fundamental frequency has been limited to a range of approximately 200 to 300 MHz, since the higher the frequency, the greater the difficulty of making crystal cuts for AT cut resonators.

Using its proprietary quartz-cutting and circuit-design technologies, Daishinku Corporation has developed the DSV753C series of VCXOs. These voltage-controlled crystal oscillators offer the excellent frequency-temperature characteristics of AT-cut resonators, are free from signal quality degradation resulting from frequency multiplication, and provide high-frequency output up to 700 MHz.

The DSV753C series in 7.0 x 5.0 x 1.8 mm size are surface-mounted voltage-controlled crystal oscillators. Output frequency is available in the range of 350 to 700 MHz, a substantial extension from the upper limit frequency of 350 MHz with conventional models. Their output signal levels support two types of differential digital signal at LVDS (DSV753CJ) and LV-PECL (DSV753CK) levels.

The new products will be exhibited at CEATEC JAPAN 2013, to be held in Makuhari Messe from October 1 to October 5, 2013 (Daishinku booth: 1A07, Hall 1).

* Source: survey by DAISHINKU CORP. valid as of September 9, 2013

<Product>
DSV753CJ / DSV753CK

<Features>
- 7050size(7.0 ×5.0 mm), 1.8mm height typ.(2.0mm max.)
- Output Frequency Range: 350 to 700 MHz
- Use of fundamental oscillation mode AT-cut crystal resonator for direct output of oscillation frequency
- Frequency output with no multiplication, eliminating spurious responses caused by fundamental frequency leakage
- Low-jitter and Low-noise
- Excellent frequency control linearity
- Supports two types of differential signal LVDS and LV-PECL

■ RoHS compliant

<Main applications>
Trunk line communication base stations, optical transmission devices, radio transmitters and receivers, digital video applications and HDTV-related equipment

<Mass Production date>
Jan., 2014

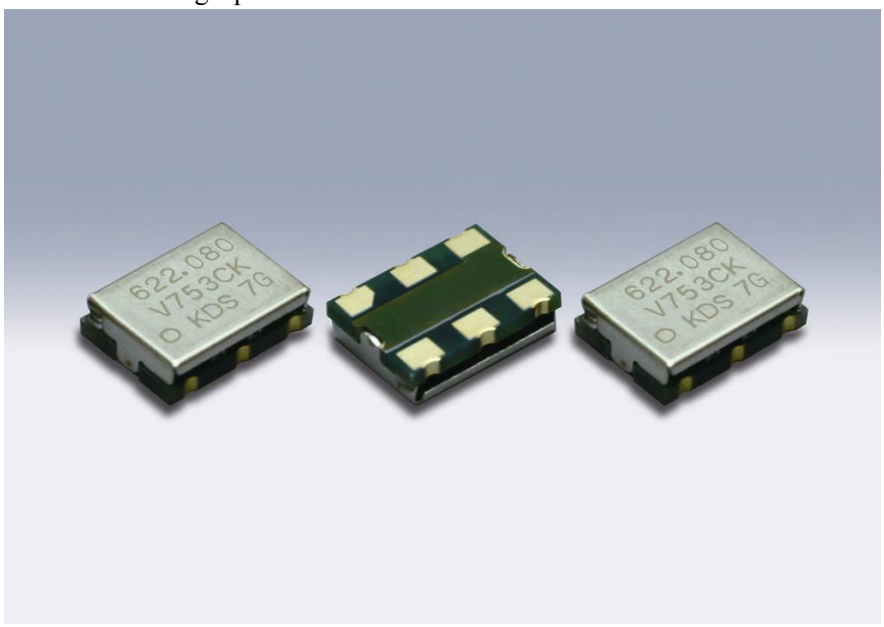
<Sample price>
7,000 yen sample are available now.

<Electrical specification>

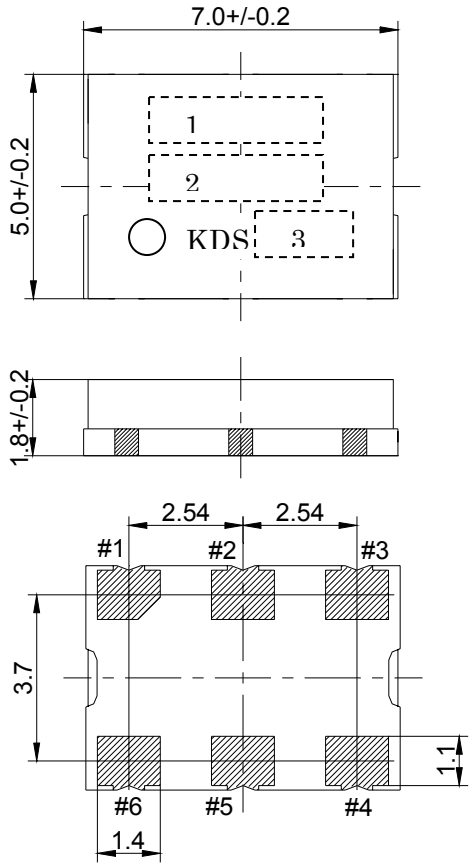
Item \ Type	Legend	DSV753CK	DSV753CJ
Output Specification	–	LV-PECL	LVDS
Output Frequency Range	f0	350MHz～700MHz	
Supply Voltage	Vcc	+3.3+/-0.165V	
Frequency Control Voltage	Vcont	+1.65+/-1.65V	
Storage Temperature Range	T_stg	-40 to +85℃	
Operating Temperature Range	T_use	-20 to +70℃	
Frequency Tolerance	f_tol	$+/-50\times10^{-6}$ max.	
Frequency Adjustment Range	f_cont	$+/-100\times10^{-6}$ min. Positive Slope	
Current Consumption	Icc	80mA max.	60mA max.
Output Load	Load	50ohm to Vcc-2V	100ohm Output-OutputN
Symmetry	SYM	45 to 55% [at outputs cross point]	
Rise and Fall Time	tr,tf	0.4ns max. [20 to 80% Output Level]	
0 Level Output Voltage	Vol	2.155V to 2.405V	–
1 Level Output Voltage	Voh	1.355V to 1.700V	–
Differential Output Voltage	V_{OD1},V_{OD2}	–	0.247 to 0.454V
Change to VOD	ΔV_{OD}	–	50mV [$\Delta V_{OD}=\|V_{OD1}-V_{OD2}\|$]
Offset Voltage	V_{OS1},V_{OS2}	–	1.125 to 1.375V
Offset to VOS	ΔV_{OS}	–	100mV [$\Delta V_{OS}=\|V_{OS1}-V_{OS2}\|$]
Phase Jitter	tpj	1ps max.(f0 offset:12kHz～20MHz)	

Consult our sales representative for other specifications.

<Product Photograph>



<Dimensions>



Pin Connections

Pin No.	Connection
#1	Vcont
#2	NC
#3	GND
#4	Output
#5	OutputN
#6	Vcc

Marking

1.Freq. [MHz]	Frequency
2.Type	J/K
3.LOT	(LOT No.)

LOT No.: (Last digit of Year) (Month)
e.g. Jan.2013 3A

Month	1	2	3	4	5	6	7	8	9	10	11	12
Code	A	B	C	D	E	F	G	H	J	K	L	M

Recommended Land Pattern

<TOP VIEW>